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Fabrication and Characteristics of Flexible Thin Film Depletion Mode Field Effect Transistor (FET) using High-κ Dielectric Nano Zirconia

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ABSTRACT

This present work focuses on preparation of high quality Zirconia (ZrO_2) thin films, a high-κ dielectric material by a modified sol-gel technique. The precursor was Zirconium (IV) Propoxide added in proper proportion with Iso Propyl Alcohol. Acetyl acetone in Iso Propyl Alcohol was used as a gelating agent. The prepared Zirconia was coated onto a glass plate and found that there was poor adhesion after firing (110°C for 4h). Hence a coating of Poly (Ethylene Terephthalate) was used before ZrO_2 film formation on a glass plate, which results in better adhesive and uniform distribution. Since it is unable to peel off, the ZrO_2/PET film is prepared and is coated on the flexible ITO PET substrate. Then, a semiconducting SWNT layer is coated above the ZrO_2/PET layer. The terminals of Source, Drain and Gate are soldered using silver paste. Thus, the field effect transistor is fabricated using high-κ dielectric ZrO_2 on a flexible PET substrate. Finally, the fabricated FET is characterized.

Index terms - Field Effect Transistor; High-κ dielectric; ITO/PET; Sol-Gel Synthesis; Thin-film; ZrO_2

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1. INTRODUCTION:

In view of the fact that the dawn of the Metal Oxide Semiconductor (MOS) Technology over 50 years ago, the SiO_2 gate oxide has been providing as the solution for scaling silicon CMOS technology. Even so, the continued SiO_2 thin dielectric gate oxide scaling is becoming extremely complicated since: (a) the gate oxide leakage increases with the decrease in SiO_2 thickness, and (b) SiO_2 also arrived at infinitesimal layer limitation point forbidding further diminution [1]. Moore's law enlarges scaling and device performance into the future, high-κ gate dielectrics based electronic devices needed for high-performance CMOS and low-power VLSI applications in the 32 nm node and beyond [2].

In addition to smooth the progress of standard Si MOS transistors, the high-κ dielectric/metal or poly Si gate combination is also important for enabling future high-performance and low gate-leakage come into sight of nanoelectronic transistors built upon non-silicon high-mobility materials, e.g. GaAs, Ge, Carbon Nanotube, and III-V substrates. The aiding of high-performance and high gate-leakage silicon and non-silicon transistor nanotechnology research via use of high-κ gate dielectrics and metal gate electrodes is endeavoured in this thesis work. Substituting the silicon dioxide gate dielectric with another high dielectric material adds complication to the industrialized process. Silicon dioxide formed by oxidizing the core silicon, certifying a uniform and high interface quality oxide [3].

As significance, improvement endeavours have focused on recovering a material with a requisitely high dielectric constant that is easily put together into a manufacturing process.

Other primary considerations include band arrangement of silicon, thin film morphology, thermal stability, and preservation of high charge carrier mobility in the channel and reduction of electrical defects in the film to film interface. Materials which received substantial attention are titanium oxide, aluminium oxide, tantalum oxide, hafnium silicate, zirconium silicate, hafnium dioxide and zirconium dioxide. It is expected that the synthesis of high–κ dielectric nanoparticles can influence its electrical properties for the fabrication of thin film depletion mode Field Effect Transistor [4]. In this work, Zirconium dioxide (ZrO_2) is chosen for the fabrication of high-κ dielectric material.

2. EXPERIMENTAL PROCEDURE AND METHODOLOGY:

The precursor was Zirconium (IV) Propoxide added in proper proportion with Iso Propyl Alcohol. Acetyl acetone in Iso Propyl Alcohol was used as a gelating agent [5]. The prepared Zirconia was coated onto a glass plate and found that there was poor adhesion after firing (110°C for 4h). Hence a coating of Polyethylene Terephthalate was used before ZrO_2 film formation on a glass plate, which results in better adhesive and uniform distribution. Since it is unable to peel off, a commercially available ITO PET substrate is taken, which is flexible. The conductive Indium-Tin Oxide coating is considered to be the gate layer of the FET. The prepared Sol-gel Zirconia is coated above the substrate, which is found to be non adhesive. So the prepared Zirconium dioxide nanoparticle is mixed with 1 wt% of PET in 10mL phenol solution and stirred well for 1hr and then a few drops is poured above the substrate and allowed to dry. This Zirconia combined with Polyethylene Terephthalate (ZrO_2/PET) stick uniformly and homogeneous to the substrate. Then, 2w/v% of CMC in distilled water is prepared with appropriate weight of CMC in appropriate volume of water. 5w/v% of SWNT in 2w/v% of CMC solution is prepared with appropriate weight of SWNT in appropriate weight of SWNT in appropriate volume of 2w/v% of CMC solution. The solution is then sonicated in ultrasonicator for 30 minutes and then in bathsonicator for 5 minutes. This sonication process is repeated four times. Then, the semiconducting layer of CNT is coated on the dielectric ZrO_2/PET layer. Finally, Source and drain terminals are soldered on the CNT layer at a distance of around 6mm using silver paste and allowed to dry overnight to dry overnight before measurements and from the conductive ITO, gate terminal is taken.

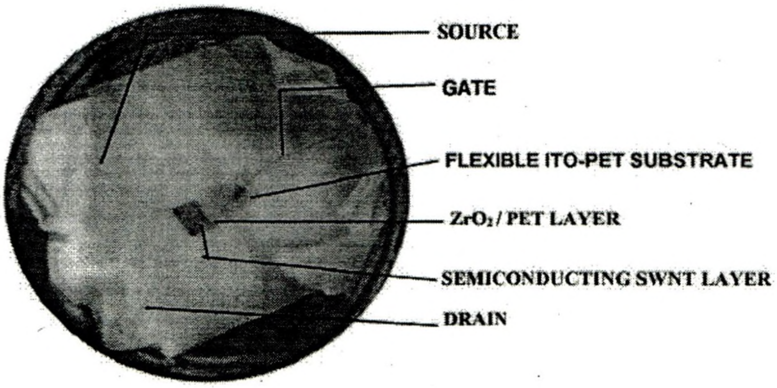

Fig. 1 Fabricated thin film FET using ZrO_2 on a flexible ITO/PET substrate

Then, I-V characteristics of the fabricated FET are measured using the NI-LABVIEW software programming for the Discrete Components Measurements.

3. SIMULATION RESULTS AND DISCUSSIONS:

The SEM image of the prepared Zirconia Nanoparticle is shown below in Fig. 2.

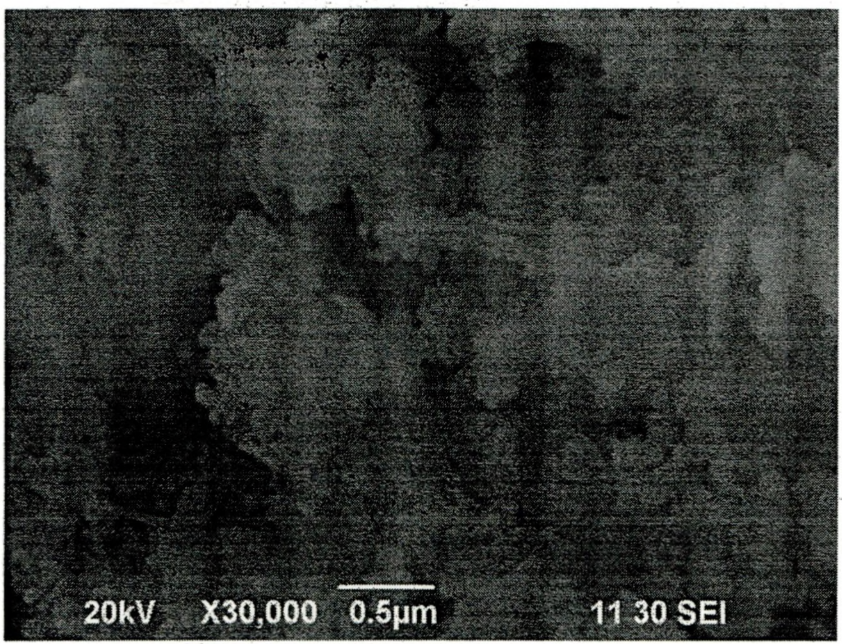

Fig. 2: SEM image of Nano Zirconia

The gate voltage is kept constant and the graph is drawn between V_{ds} and I_d for V_{ds} = 0V to 10 V. At constant gate voltage, the V_{ds} Vs I_{ds} is drawn to obtain its knee voltage and to study the switching mode of the transistor. When the gate voltage is 1.993V, the knee voltage is found to be 5.3046V. Therefore, when the gate voltage is applied to 1.993V, I_{OFF} state will be switched into I_{ON} state to 5.3046V and vice versa. Similarly, the device operates for the various gate voltages. Thus, this fabricated field effect transistor act perfectly as a normal operation of a transistor.

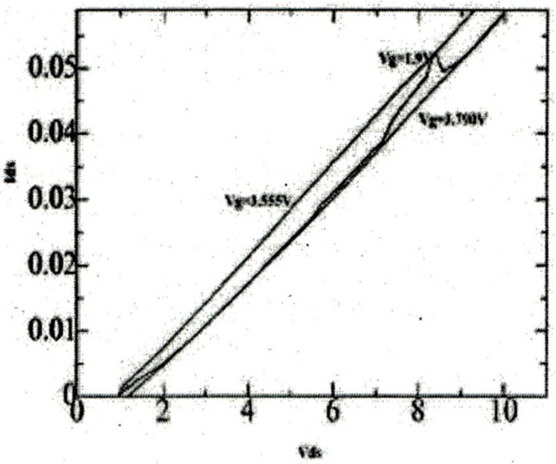

Fig. 3: VI characteristics of V_{ds} (0V-10V) Vs I_{ds} at constant V_g

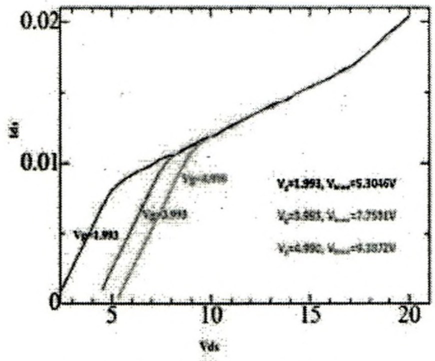

Fig. 4: VI Characteristics between V_{ds} (0-20V) Vs I_{ds}, at constant V_g

4. CONCLUSION:

In summary, the field effect transistor (FET) using high-κ dielectric ZrO_2 on a flexible ITO PET substrate is fabricated. Then, the flexible thin film fabricated field effect transistor is characterized at room temperature. The IV characteristics are hence studied, in which the threshold voltage is 0.46V. It is hence found to be lesser than the threshold voltage of conventionally used SiO_2 dielectric gate FETs. Hence, the switching speed is faster than the SiO_2 dielectric gate FETs. The future work will be done in double gate (FinFET) field effect transistor using ZrO_2 which is a high-κ dielectric material [6].

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Dr. Nalini B. received her B.Sc. (Physics) from Bharathiar University (India) in 1989 and M.Sc. (Physics) from Bharathiar University (India), in 1991. She received Ph.D. from Bharathiar University (India), in 1997. Her area of specialization includes Solid State Ionics, Nanotechnology and Gas Sensors. She is now Assistant professor in Physics Department, Avinashilingam University for Women, Coimbatore. She is life member of Indian Society of Solid State Ionics, Indian Society for Technical Education, Society of Magnetic Materials and active member of several technical associations. She has published many papers in international journals. She was awarded with Senior Research Fellowship awarded by Council of Scientific and Industrial Research, Government of India (1995 – 1996) and also STA Fellowship awarded by Japan Industrial Science and Technology, Science and Technology Agency, Japan (Jan. 2000 – Jan. 2002).

Dr. D. Nirmal received his B.E. (Electrical and Electronics Engineering) from the Anna University, Chennai in 2005 and M.E. from Karunya University, in 2007. He received Ph.D. from Anna University, Coimbatore. He is currently focusing on Novel MOS devices for ULSI applications: Transistors with high-k dielectrics. He is now Assistant professor in Electronics and Communication Engineering Department, Karunya University. He is a member of VLSI Society of India (VSI), AMIETE, MSSI (Member of Semiconductor Society of India), life member of Indian Society of Technical Education (ISTE) and active member of several technical associations. He has published many papers in international journals.

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