Avinashilingam Institute for Home Science and Higher Education for Women

Deemed to be University Estd. u/s 3 of UGC Act 1956, Category 'A' by MHRD (now MoE)
Re-accredited with 'A++' Grade by NAAC. CGPA 3.65/4, Category I by UGC
Coimbatore - 641 043, Tamil Nadu, India

Bachelor's Degree Arrear Examination – May 2025
I Semester

Batch : 2023 | **Time: 3 Hours**
Major : Computer Science | **Max. Marks: 100**

23BCSC02 Computer System Architecture

Course Outcomes:

CO1: Apply Boolean Logic in circuit design with gates and other digital hardwares
CO2: Distinguish the application of various micro-operations in Register Transfer Language.
CO3: Handle the various parameters related to instruction execution.
CO4: Understand the control unit implementation and CPU instruction handling.
CO5: Appraise the various information storage - retrieval concepts and I/O transfer methods

Part A
Choose the correct answer **10 x 1 = 10**

1. Which of the following is Universal Gate? CO1 K1
   a. NAND gate b. OR gate
   c. AND gate d. Ex-OR gate

2. A + A.B = ? CO1 K3
   a. B b. A.B
   c. A d. A+B

3. RTL stands for: CO2 K1
   a. Random transfer language b. Register transfer language
   c. Arithmetic transfer language d. All of these

4. Which micro-operations carry information from one register to another? CO2 K2
   a. Register transfer b. Arithmetic
   c. Logical d. All of these

5. The fetched instruction is loaded into a register in the processor known as the CO3 K3
   a. Memory b. kernel
   c. Instruction register (IR) d. memory registers

6. The operation is specified by a binary code, known as the CO3 K1
   a. operation code or opcode b. source operand reference
   c. result operand reference d. None of them

7. A set of microinstructions for a single machine instruction is called _____ CO4 K1
   a. Program b. Command
   c. Micro program d. Micro command

8. The memory that reduces the total execution time of the program is _____ CO4 K2
   a. RAM b. ROM
   c. Cache d. Auxiliary memory

9. In DMA, transfers are performed by a control circuit called as _____ CO5 K2
   a. Device interface b. DMA controller
   c. Data controller d. Overlooker

10. Memory unit accessed by content is called CO5 K2
   a. Read only memory b. Programmable Memory
   c. Virtual Memory d. Associative Memory

Part B 5 x 6 = 30

Answer ALL Questions

Each answer should not exceed 400 words or two pages

11. a. Write short notes on complements.	CO1 K1
(or)	
11. b. State and prove De-Morgans theorems.	CO1 K2
12. a. Write short notes on Register Transfer Language.	CO2 K2
(or)	
12. b. What are arithmetic micro-operations? Discuss.	CO2 K1
13 a. List the Registers for the basic computer and give their basic functions.	CO3 K1
(or)	
13.b. Write on short note on memory reference instructions.	CO3 K2
14.a. Discuss the various types of instruction formats with examples.	CO4 K2
(or)	
14.b. Differentiate between RISC and CISC.	CO4 K1
15.a. Describe Input/output Interface in detail.	CO5 K1
(or)	
15.b. Explain in detail about Memory Hierarchy with neat diagram.	CO5 K2

Part C 5 x 12 = 60

Answer ALL questions

Each answer should not exceed 800 words or four pages

16. a. Define Logic Gate and discuss various gates with diagram and their truth table.	CO1 K2
(or)	
16. b. Draw the logic diagram of full adder and explain in detail.	CO1 K1
17. a. Discuss bus and memory transfer in detail.	CO2 K1
(or)	
17.b. Explain shift micro-operation.	CO2 K2
18.a. Briefly discuss on instruction cycle.	CO3 K1
(or)	
18. b. Write on Input-Output and interrupts.	CO3 K2
19.a. Explain stack organization of CPU in detail.	CO4 K2
(or)	
19. b. Explain data transfer and manipulation instruction with example.	CO4 K2
20.a. What is DMA? Explain the working of DMA in detail.	CO5 K2
(or)	
20. b. Discuss the various mapping schemes used in cache memory.	CO5 K3

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