Avinashilingam Institute for Home Science and Higher Education for Women

(Deemed to be University under Category 'A' by MHRD, Estd. u/s 3 of UGC Act 1956)
Re-accredited with 'A+' Grade by NAAC. Recognised by UGC Under Section 12B
Coimbatore - 641 043, Tamil Nadu, India

Bachelor's Degree Examination –November 2019
III Semester

Class : II UG **Time: 3 hours**
Major : Computer Applications **Max. Marks: 100**

18BCAC09-Computer Organization and Architecture

Part A **10 x 1 = 10**

Choose the correct answer

1. The device which is used to connect a peripheral to bus is known as _____
   (A) control register (B) interface (C) communication protocol (D) none of these

2. A CPU handles interrupt by executing interrupt service subroutine _____.
   (A) by checking interrupt register after execution of each instruction
   (B) by checking interrupt register at the end of the fetch cycle
   (C) whenever an interrupt is registered
   (D) by checking interrupt register at regular time interval

3. In _____ method, the word is written to the block in both the cache and main memory, in parallel.
   (A) Write through (B) Write back (C) Write protected (D) Direct mapping

4. _____ is not a component of Memory tube display.
   (A) Flooding gun (B) Collector (C) Ground (D) Liquid Crystal

5. Register renaming is done in pipelined processors
   (A) as an alternative to register allocation at compile time
   (B) for efficient access to function parameters and local variables
   (C) to handle certain kinds of hazards
   (D) as part of address translation

6. Micro program is _____.
   (A) the name of a source program in microcomputers
   (B) set of micro instructions that defines the individual operations in response to a machine-language instruction
   (C) a primitive form of macros used in assembly language programming
   (D) a very small segment of machine code

7. _____ of ROM needed to implement a 4 bit multiplier
   (A) 64 bits (B) 128 bits (C) 1 Kbits (D) 2 Kbits

8. More than one word are put in one cache block to _____.
   (A) exploit the temporal locality of reference in a program
   (B) exploit the spatial locality of reference in a program
   (C) reduce the miss penalty
   (D) none of the above

9. _____ addressing modes permits relocation without any change whatsoever in the code.
(A) Indirect addressing (B) Indexed addressing
(C) Base register addressing (D) PC relative addressing

10. _____ is an interrupt according to temporal relationship with system clock.
(A) Maskable interrupt (B) Periodic interrupt
(C) Division by zero (D) Synchronous interrupt

Part B **5 x 6 = 30**

Answer ALL questions
Each answer should not exceed 400 words or two pages

11.a. Write down the different basic operations of Computers.

(or)

11.b. Distinguish between Multiprocessors and Multi Computers.

12.a. Explain the Arithmetic Operations in Machine programs.

(or)

12.b. Illustrate subroutine in Machine instructions

13.a. Summarize the steps involved in the Micro programmed control.

(or)

13.b. What is meant by Hazard in pipelining? Brief its types.

14.a. Write short notes on the Performance considerations of Memory .

(or)

14.b. What is Cache Memory? Illustrate the mapping functions of cache memory with neat diagrams.

15.a. List out the I/O addressing in a computer organization.

(or)

15.b. What are the functions of an I/O interface?

Part C **5 x 12 = 60**

Answer ALL questions
Each answer should not exceed 800 words or four pages

16.a. List out the Functional units of Computer with detailed explanations.

(or)

16.b. Summarize the Bus structure with suitable example.

17.a. Explain in detail the Input/Output operations of assembly Language.

(or)

17.b. Illustrate the different addressing modes found in the processors with examples.

18.a. Summarize the concepts of Multiple Bus Organization in detail.

(or)

18.b. Explain in detail the basics of pipelining and how it is used in computers to achieve high performance.

19.a. Illustrate the Memory Hierarchy and Parameters in detail.

(or)

19.b. What is Cache Memory? Illustrate the mapping functions of Cache memory with neat diagrams.

20.a. List the Input/Output interface with suitable example.

(or)

20.b. Explain with diagram, the working of Interrupts.

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Set-2

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18BCAC09-Computer Organization and Architecture

Part A **10 x 1 = 10**

Choose the correct answer

1. The _____ is used to hold the address of the location.
   (A) MAR (memory address register) **(B)** Interrupt service register
   (C) Interrupt mask register **(D)** MDR(memory data register) CO1K1

2. A collection of wires that connects several devices is called a _____.

   (A) Bus **(B)** Star **(C)** Ring **(D)** LAN CO1K2

3. The register that stores the bits required to mask the interrupts is _____.
   (A) Status register **(B)** Interrupt service register **(C)** Interrupt mask register
   (D) Interrupt request register CO2K2

4. The search concept used in associative memory is _____.
   (A) Parallel search **(B)** Sequential search **(C)** Binary search **(D)** Selection search
   CO2K1

5. Register renaming is done in pipelined processors
   (A) as an alternative to register allocation at compile time
   (B) for efficient access to function parameters and local variables
   (C) to handle certain kinds of hazards **(D)** as part of address translation CO3K2

6. The amount of ROM needed to implement a 4 bit multiplier is _____.
   (A) 64 bits **(B)** 128 bits **(C)** 1 Kbits **(D)** 2 Kbits CO3K1

7. Relative mode of addressing is most relevant to _____.
   (A) co-routines **(B)** position-independent code **(C)** shareable code
   (D) interrupt handerls CO4K1

8. _____ is not used for mapping process in cache memory.
   (A) Associative mapping **(B)** Direct mapping
   (C) Set-Associative mapping **(D)** Segmented – page mapping CO4K2

9. MOS is a Computer Chip on the motherboard, which is_____.
   (A) RAM **(B)** ROM **(C)** EPROM **(D)** Auxillary storage CO5K1

10. On receiving an interrupt from an I/O device,the CPU

    (A) Halts for a predetermined time
    (B) Branches off to the interrupt service routine after completion of the current instruction
    (C) Branches off to the interrupt service routine immediately
    (D) Hands over control of address bus and data bus to the interrupting device CO5K2

Part B **5 x 6 = 30**

Answer ALL questions
Each answer should not exceed 400 words or two pages

11.a. Classify the different types of Computers with a brief description. CO1K1

(or)

11.b. Write down the uses of Multiprocessors. CO1K2

12.a. Explain with example how the numbers are represented using
1) 1's complement 2) 2's complement CO2K2

(or)

12.b. Illustrate the Stacks and Queues in details. CO2K1

13.a. List out the steps involved in the execution of a complete instruction. Draw the flow of instruction cycle. CO3K1

(or)

13.b. Briefly explain the Micro program Sequencing its example. CO3K2

14.a. Write short notes on the following with neat diagrams wherever necessary
1)Memory Hierarchy 2)Performance considerations of Memory CO4K1

(or)

14.b. What is Memory Mapping? Illustrate the memory mapping functions with neat diagrams. CO4 K2

15.a. Explain the mode of data transfer in a computer organization. CO5K1

(or)

15.b. What are the functions of an I/O interface? CO5K1

Part C **5 x 12 = 60**

Answer ALL questions
Each answer should not exceed 800 words or four pages

16.a. Summarize the Generations of Computers. List of their Significance and Applications with detailed explanations. CO1K2

(or)

16.b. Distinguish between Multiprocessors and Multi computers in detail. CO1K3

17.a. Explain in detail the different Instruction types and Instruction Sequencing. CO2K1

(or)

17.b. Illustrate the different addressing modes and Subroutines. CO2K2

18.a. Summarize the concepts of Micro programmed Control. CO3K1

(or)

18.b. Explain in detail the basics of Data Hazards and how it is used in computers to achieve high performance. CO3K2

19.a. Explain in detail the Memory system and Concepts. CO4K1

(or)

19.b. What is Cache Memory? Illustrate the mapping functions of Cache memory with neat diagrams. CO4K2

20.a. Summarize the working of Direct Memory Access. CO5K1

(or)

20.b. Explain with diagram, the working of I/O Interfaces. CO5K2

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