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**Avinashilingam Institute for Home Science and Higher Education for Women**
Deemed to be University Estd. u/s 3 of UGC Act 1956, Category A by MHRD (now MoE)
Re-accredited with A++ Grade by NAAC. CGPA 3.65/4, Category I by UGC
Coimbatore - 641043, Tamil Nadu, India

## Bachelor's Degree Examination – November 2025
## I Semester

**Class : I UG**
**Major : Computer Science**

**Time : 3 Hours**
**Max. Marks: 100**

## 23BCSC02 Computer System Architecture

**Course Outcomes:**
At the end of the course, students will:
CO1: Apply Boolean Logic in circuit design with gates and other digital hardwares
CO2: Distinguish the application of various micro-operations in Register Transfer Language.
CO3: Handle the various parameters related to instruction execution.
CO4: Understand the control unit implementation and CPU instruction handling.
CO5: Appraise the various information storage - retrieval concepts and I/O transfer methods

### Part A — 10 x 1 = 10
### Choose the Correct Answer

1. The binary equivalent of the decimal number 25 is _____
   a. 11000 b. 11001 c. 10101 d. 10011 — CO1 K1

2. The circuit that stores binary information is called_____
   a. Multiplexer b. Decoder c. Flip-Flop d. Encoder — CO1 K2

3. Which micro-operation performs bitwise AND? — CO2 K1
   a. AND operation b. Transfer operation
   c. Shift operation d. Add operation

4. Shift micro-operations are used for:
   a. Arithmetic calculations b. Logical operations
   c. Data movement d. Bit manipulation — CO2 K2

5. What is the purpose of the timing and control unit?
   a. Data storage b. Synchronization of operations
   c. Memory management d. Arithmetic processing — CO3 K3

6. Input-output operations are usually controlled by _____ — CO3 K2
   a. Program Counter b. ALU
   c. Control Unit d. I/O Control Unit

7. RISC architecture uses _____
   a. Complex instructions b. Fewer instructions
   c. Slower execution d. Stack-based memory — CO4 K2

8. Stack organization is mainly used in _____
   a. RISC b. Pipelining
   c. Subroutine calls d. Control hazards — CO4 K1

9. The main memory communicates with the CPU via _____
   a. I/O bus b. Control bus
   c. Memory bus d. Data lines only — CO5 K2

10. DMA stands for_____
    a. Direct Memory Access b. Dual Memory Architecture
    c. Data Management Architecture d. Data Memory Access — CO5 K1

## Part B — 5 x 6 = 30

**Answer ALL questions**

**Each answer should not exceed 400 words or two pages**

| | | |
|---|---|---|
| 11.a. | Examine the Boolean algebra laws applied in simplifying logic circuits. | CO1 K1 |
| | (or) | |
| 11.b. | Describe the error detection codes used in digital systems. | CO1 K2 |
| 12.a. | Illustrate the basic components of register transfer language. | CO2 K3 |
| | (or) | |
| 12.b. | Summarize the arithmetic micro-operations with example. | CO2 K2 |
| 13.a. | Explain the instruction cycle with timing and control signals. | CO3 K3 |
| | (or) | |
| 13.b. | Identify the working of input-output and interrupt handling mechanisms. | CO3 K4 |
| 14.a. | Evaluate the general register organization with diagram. | CO4 K5 |
| | (or) | |
| 14.b. | Highlight the general architecture of a RISC processor. | CO4 K4 |
| 15.a. | Appraise the working and advantages of cache memory. | CO5 K5 |
| | (or) | |
| 15.b. | Explain the I/O interface and data transfer techniques. | CO5 K4 |

## Part C — 5 x 12 = 60

**Answer ALL questions**

**Each answer should not exceed 800 words or four pages**

| | | |
|---|---|---|
| 16.a. | Enumerate the working of Basic logic gates with their truth tables. | CO1 K1 |
| | (or) | |
| 16.b. | Compare and construct the fixed-point and floating-point representation. | CO1 K2 |
| 17.a. | Discover the various shift micro-operations with example. | CO2 K3 |
| | (or) | |
| 17.b. | Estimate the operations of memory transfer and bus transfer. | CO2 K2 |
| 18.a. | Examine the role of various computer registers in instruction execution. | CO3 K3 |
| | (or) | |
| 18.b. | Draw and explain the design of a basic computer with components. | CO3 K4 |
| 19.a. | Assess the handling of data hazards and control hazards. | CO4 K5 |
| | (or) | |
| 19.b. | Discriminate the hardwired and micro-programmed control units. | CO4 K5 |
| 20.a. | Conclude the types and functions of high speed memories. | CO5 K4 |
| | (or) | |
| 20.b. | Generalize the system performance of instruction-level parallelism. | CO5 K5 |

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