Avinashilingam Institute for Home Science and Higher Education for Women

(Deemed to be University under Category 'A' by MHRD, Estd. u/s 3 of UGC Act 1956)
Re-accredited with 'A+' Grade by NAAC. Recognised by UGC Under Section 12B
Coimbatore - 641 043, Tamil Nadu, India

Bachelor's Degree Examination – June / July 2021
II Semester

Class : I UG **Time : 3 Hours**
Major : Information Technology **Max. Marks : 100**

18BITC05 Digital Fundamentals Architecture

Part A **10 x 1 = 10**
Choose the Correct Answer

1. The input – output relationship of the binary variable for each gate can be represented in tabular form by a CO1K2
   a. maptable b. input table c. truth table d. gate table

2. BCD stands for CO1K1
   a. Binary Coded Decimal b. Beta Coded Decimal
   c. Brand Code Dot d. Binary Code Dot

3. An _____ is a digital circuit that performs the inverse operation of a decoder. CO2K2
   a. decoder b. barcoder c. encoder d. scanner

4. _____ is a systematic method of simplifying and modifying switching expressions. CO2K1
   a. K – Map b. N – Map c. S – Map d. T – Map

5. The stack pointer register that holds the address for the stack is called a _____ because its value always points at the top item in the stack. CO3K2
   a. stack register b. stack pointer c. register pointer d. cache pointer

6. One – address instruction use and implied _____ register for all data manipulation. CO3K1
   a. stack b. transcriptor c. resilence d. accumulator

7. The _____ bus consists of data lines, address lines, and control lines. CO4K2
   a. i/o b. storage c. internal d. external

8. A _____ takes over the buses to manage the transfer directly between the I/O device and memory. CO4K1
   a. memory bus b. data bus c. dma d. i/o bus

9. A special very high speed memory called a _____ is sometimes used to increase the speed of processing by marking current programs and data avail to the CPU at a rapid rate. CO5K1
   a. associative b. cache memory
   c. auxiliary memory d. secondary memory

10. An address in main memory is called CO5K1
   a. physical b. logical address
   c. temporary address d. virtual address

Part B **5 x 6 = 30**

Answer ALL questions
Each answer should not exceed 400 words or two pages

11.a. Demonstrate the conversion of decimal number $(115)_{10}$ to hexadecimal number. CO1K3

(or)

11.b. Illustrate the working of NOR gate and NAND gate with suitable diagram. CO1K4

12.a. Discuss the Properties of Boolean Algebra. CO2K2

(or)

12.b. Explain briefly construction and properties of Karnaugh map. CO2K3

13.a. Examine about the working of control word in general register organization. CO3K3

(or)

13.b. Illustrate the different types of instruction formats with suitable example. CO3K3

14.a. Compare I/O bus versus Memory Bus. CO4K4

(or)

14.b. Analyse the working of strobe control and handshaking with neat figures. C04K4

15.a. Describe the memory hierarchy in memory organization. CO5K2

(or)

15.b. Evaluate the associative mapping and direct mapping of cache memory organization. CO5K4

Part C **5 x 12 = 60**

Answer ALL questions
Each answer should not exceed 800 words or four pages

16.a. Apply the steps to CO1K3

i. Convert $(444.456)_{10}$ to an octal number.
ii. Convert $(120)_8$ to decimal number.
iii. Convert $(53.625)_{10}$ to an equal binary number.
iv. Convert $(A3BH)_{16}$ to decimal number.

(or)

16.b. Explain in detail the procedure for the design of combinational Half Adder and full adder circuits. CO1K2

17.a. Analyze in detail sum of products and product of sum. CO2K3

(or)

17.b. Illustrate the S-R and J-K flip-flop and draw the state diagram and characteristic equation.

18.a. Analyze the various data transfer and data manipulation instruction of CPU. CO3K4

(or)

18.b. Evaluate the different addressing modes of an instruction with a numerical example. CO3K4

19.a. Examine the different types of Priority interrupts in detail. CO4K3

(or)

19.b. Discuss in detail about the benefits of Direct Memory Access. CO4K2

20.a. Explain the working of Associative Memory. CO5K3

(or)

20.b. Analyse the concept of Virtual Memory Organization in detail. CO5K4

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